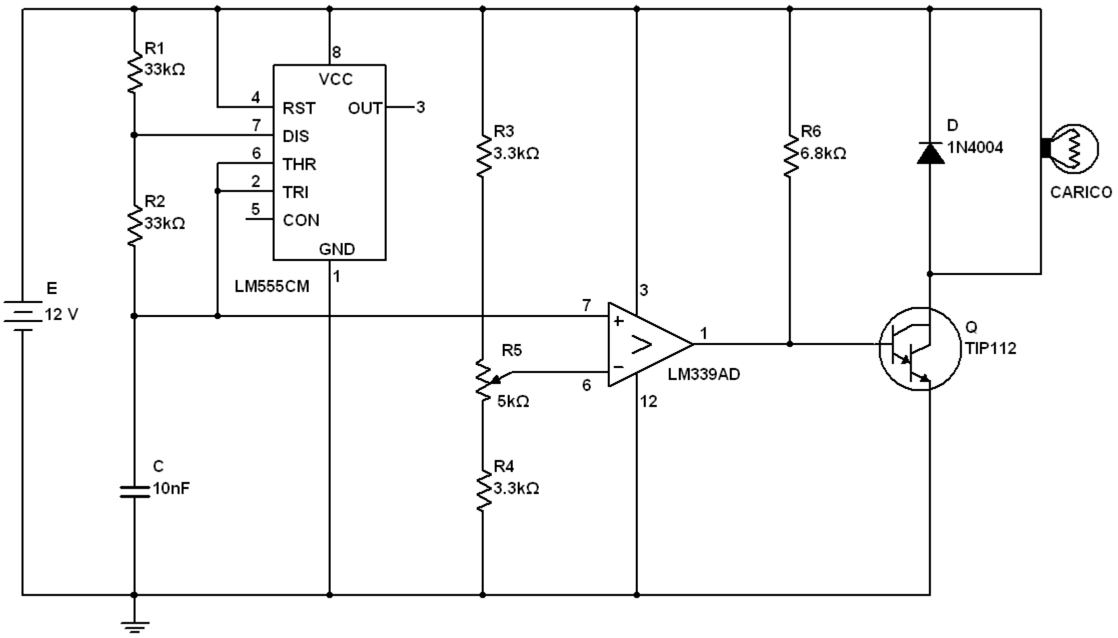
Classe	*5^a Elettronici*
Materia	*T.D.P.*
Argomento	*Controllo di Potenza*

Controllo di potenza in continua con transistor in commutazione pilotato da un segnale PWM

Vogliamo costruire un circuito che ci permetta di controllare la potenza di un carico alimentato da una batteria tramite un transistor fatto funzionare alternativamente in conduzione e interdizione.

Lo schema utilizzato è il seguente:



La parte di controllo è costituita da un oscillatore realizzato con un LM555 in configurazione astabile e da un comparatore LM339 mentre la parte di potenza utilizza il BJT Darlington TIP112.

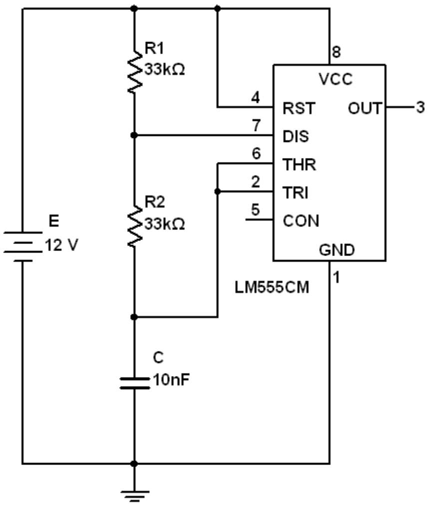
Il timer LM555 nella configurazione indicata oscilla grazie alla carica e scarica del condensatore *C* in un intervallo di tensione compreso tra:

$$\frac{1}{3}E < V_C(t) < \frac{2}{3}E$$

Nel nostro caso essendo

$$E = 12\text{V}$$

si ha



$$4 < V_C(t) < 8 \quad \mathrm{V}$$

L’LM555 gestisce la carica e scarica del condensatore rilevando la tensione ai suoi capi grazie ai pin 6 e 2 (*threshold* e *trigger*) aprendo e chiudendo alternativamente un interruttore al suo interno che fa capo al pin 7 (*discharge*).

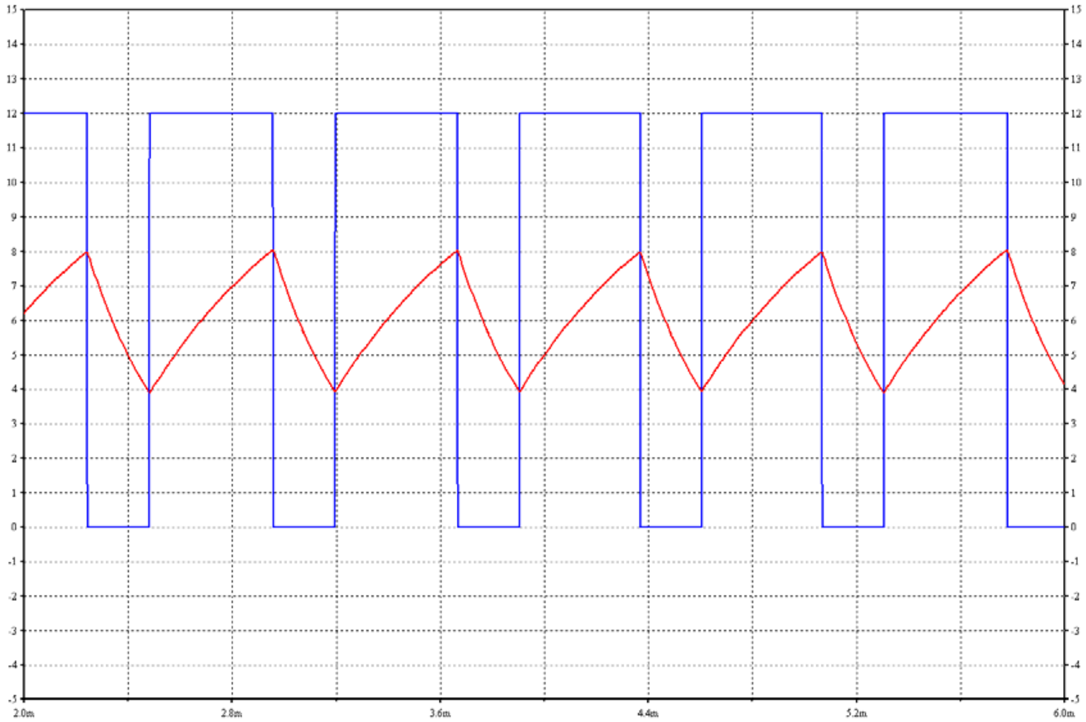
Nel passaggio da 4 V a 8 V il condensatore si carica tramite la batteria attraverso le due resistenze R_1 ed R_2 in un tempo T_1 pari a:

$$T_1 = (R_1 + R_2) C \log_e 2$$

Nel passaggio da 8 V a 4 V il condensatore si scarica attraverso la sola resistenza R_2 sul piedino 7 del LM555 che si porta a massa in un tempo pari a:

$$T_2 = R_2 C \log_e 2$$

Nella fase di carica il pin 3 (*output*) si porta a livello logico alto (12 V) mentre in quella di scarica a livello logico basso (~0 V).



Nel caso in esame sul pin 3 di uscita si ha quindi un’onda rettangolare avente una frequenza:

$$f=\frac{1}{T}=\frac{1}{T_1+T_2}=\frac{1}{\left(R_1+2R_2\right)C\log_e 2}=\frac{1}{3\cdot 33\cdot 10^3\cdot 10\cdot 10^{-9}\cdot\log_e 2}\cong 1457\text{Hz}$$

e un duty-cycle:

$$\text{d.c.}_{(\%)}=\frac{T_1}{T}=\frac{T_1}{T_1+T_2}=\frac{R_1+R_2}{R_1+2R_2}=\frac{2}{3}\cong 66.7\%$$

Il nostro obiettivo è però quello di avere un’onda rettangolare con duty-cycle variabile in un intervallo compreso tra 0 e il 100%.

Per fare questo si usa la tensione ai capi del condensatore e la si confronta con una tensione costante nel comparatore LM339 che in uscita darà il valore alto solo quando la tensione al morsetto positivo supererà quella di riferimento.

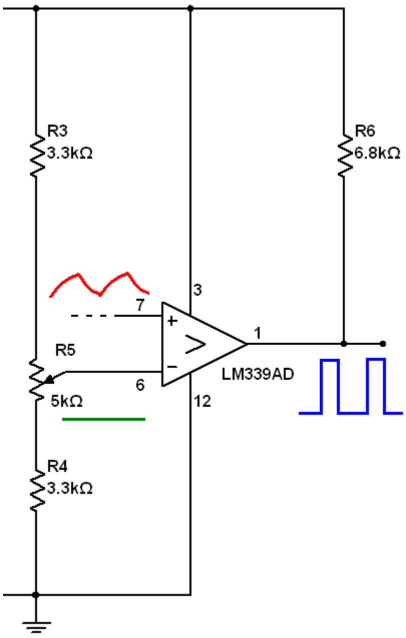
La tensione di confronto all’ingresso negativo del comparatore è ottenuta tramite un partitore costituito dalle resistenze R_3 ed R_4 e dal trimmer R_5.

Con i valori scelti si ha:

$$V_{-\min}=\frac{R_4}{R_3+R_4+R_5}E=\frac{3.3\cdot 10^3}{(3.3+3.3+5)\cdot 10^3}E=12\frac{3.3}{11.6}\cong 3.41<4=V_{+\min}$$

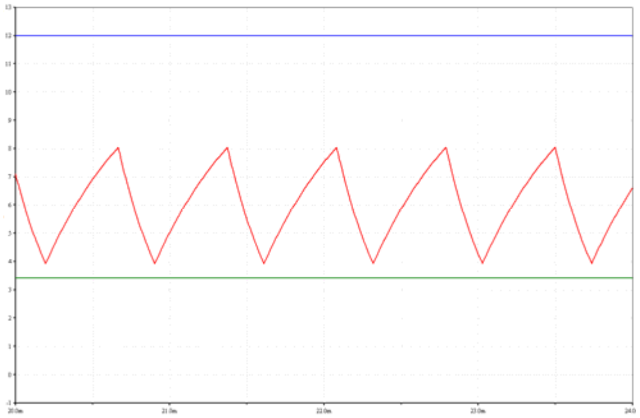
e

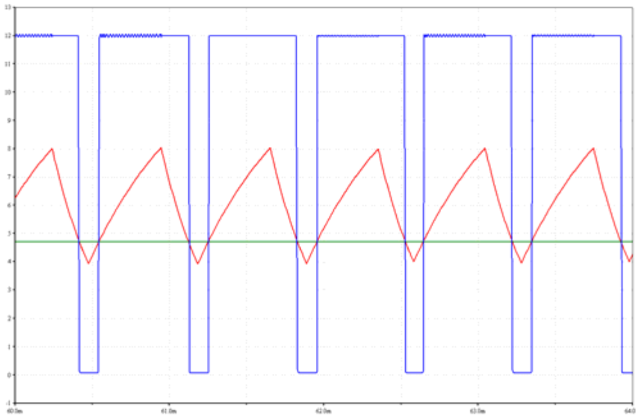
$$V_{-\max}=\frac{R_4+R_5}{R_3+R_4+R_5}E=\frac{(3.3+5)\cdot 10^3}{(3.3+3.3+5)\cdot 10^3}E=12\frac{8.3}{11.6}\cong 8.59>8=V_{+\max}$$

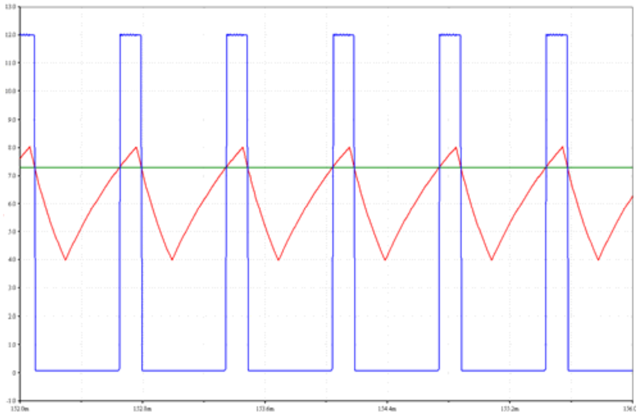


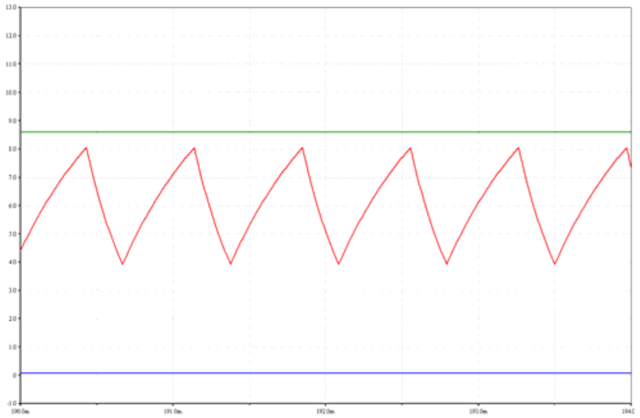
Pertanto al variare del trimmer, la tensione sull’ingresso negativo varia in un intervallo più ampio rispetto a quella del condensatore che è limitata tra 4 e 8 V.

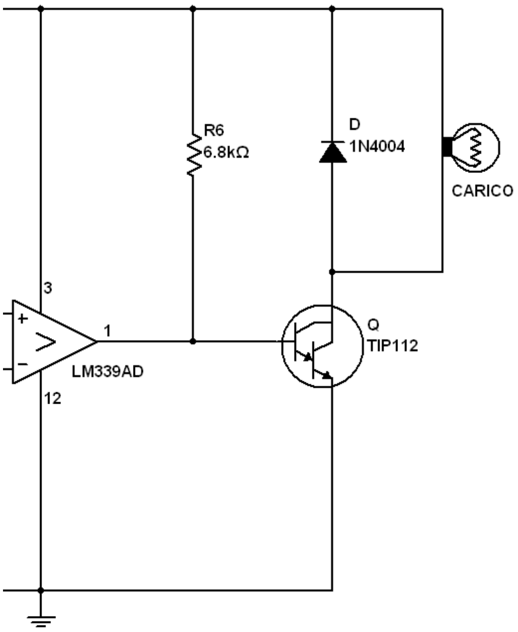
Le figure successive mostrano l’andamento della tensione a vuoto all’uscita del comparatore per diversi valore di regolazione del trimmer dalla minima alla massima resistenza (L’LM339 ha un’uscita open-collector e richiede una resistenza di pull-up).


13
12
11
10
9
8
7
6
5
4
3
2
1
0
-1
20.0m
21.0m
22.0m
23.0m
24.0


13
12
11
10
9
8
7
6
5
4
3
2
1
0
-1
60.0m
61.0m
62.0m
63.0m
64.0


13.0
12.0
11.0
10.0
9.0
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0
-1.0
152.0m
152.8m
153.6m
154.4m
155.2m
156.


13.0
12.0
11.0
10.0
9.0
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0
-1.0
190.0m
191.0m
192.0m
193.0m
194.



Collegata all'uscita del comparatore vi è infine la parte di potenza costituita da un transistor Darlington ad elevato guadagno (valori di h_{FE} compresi tra 500 e 1000) ed una corrente di collettore $I_{C\max}$=2 A.

La resistenza di base del TIP112 è stata calcolata per avere un margine di sicurezza sul dispositivo, infatti quando il comparatore si trova nello stato OFF si ha:

$$I_B = \frac{E - V_{BE0}}{R_6} = \frac{12 - 2.8}{6.8 \cdot 10^3} = 1.35\,\text{mA}$$

pertanto risulta nella peggiore delle ipotesi:

$$I_C = h_{FE\max} I_B = 1000 \cdot 1.35 \cdot 10^{-3} = 1.35\text{A}$$

che è minore della massima corrente di collettore ammessa dal BJT.

Per concludere è stato inserito sul collettore del TIP112 il diodo 1N4004 che serve ad utilizzare il circuito anche con carichi induttivi come motori in corrente continua.

Datasheets allegati:

- LM555
- LM339
- TIP112

LM555/NE555/SA555

Single Timer

Features

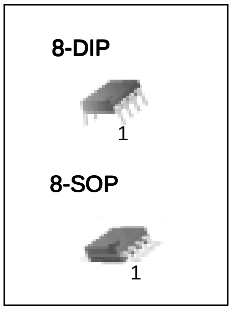
- High Current Drive Capability (200mA)
- Adjustable Duty Cycle
- Temperature Stability of 0.005%/°C
- Timing From µSec to Hours
- Turn off Time Less Than 2µSec

Applications

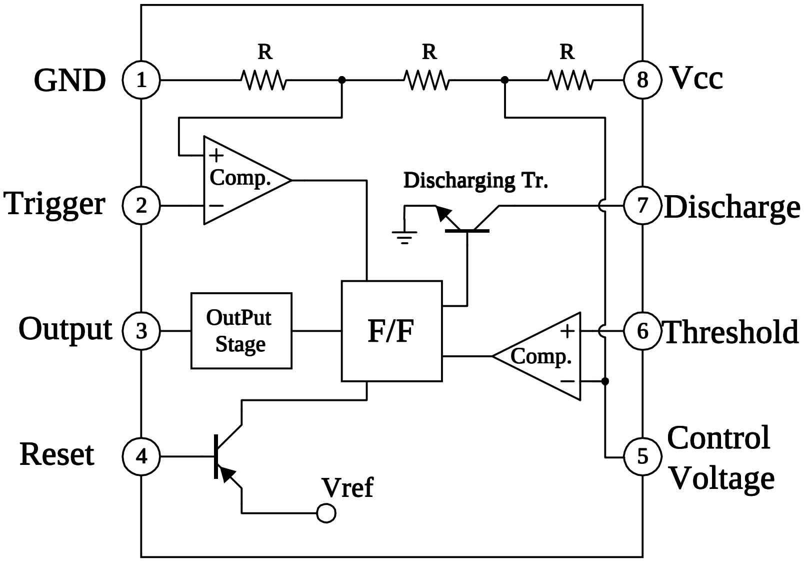
- Precision Timing
- Pulse Generation
- Time Delay Generation
- Sequential Timing

Description

The LM555/NE555/SA555 is a highly stable controller capable of producing accurate timing pulses. With a monostable operation, the time delay is controlled by one external resistor and one capacitor. With an astable operation, the frequency and duty cycle are accurately controlled by two external resistors and one capacitor.



Internal Block Diagram



Absolute Maximum Ratings (T_A = 25°C)

Parameter	**Symbol**	**Value**	**Unit**
Supply Voltage	V_{CC}	16	V
Lead Temperature (Soldering 10sec)	T_{LEAD}	300	°C
Power Dissipation	P_D	600	mW
Operating Temperature Range LM555/NE555 SA555	T_{OPR}	0 ~ +70 -40 ~ +85	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

Electrical Characteristics

(T_A = 25°C, V_{CC} = 5 ~ 15V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	-	4.5	-	16	V
Supply Current (Low Stable) (Note1)	I_{CC}	V_{CC} = 5V, $R_L = \infty$	-	3	6	mA
		V_{CC} = 15V, $R_L = \infty$	-	7.5	15	mA
Timing Error (Monostable) Initial Accuracy (Note2) Drift with Temperature (Note4) Drift with Supply Voltage (Note4)	ACCUR Δt/ΔT $\Delta t/\Delta V_{CC}$	R_A = 1kΩ to100kΩ C = 0.1μF	-	1.0 50 0.1	3.0 0.5	% ppm/°C %/V
Timing Error (Astable) Intial Accuracy (Note2) Drift with Temperature (Note4) Drift with Supply Voltage (Note4)	ACCUR Δt/ΔT $\Delta t/\Delta V_{CC}$	R_A = 1kΩ to 100kΩ C = 0.1μF	-	2.25 150 0.3	-	% ppm/°C %/V
Control Voltage	V_C	V_{CC} = 15V	9.0	10.0	11.0	V
		V_{CC} = 5V	2.6	3.33	4.0	V
Threshold Voltage	V_{TH}	V_{CC} = 15V	-	10.0	-	V
		V_{CC} = 5V	-	3.33	-	V
Threshold Current (Note3)	I_{TH}	-	-	0.1	0.25	μA
Trigger Voltage	V_{TR}	V_{CC} = 5V	1.1	1.67	2.2	V
		V_{CC} = 15V	4.5	5	5.6	V
Trigger Current	I_{TR}	V_{TR} = 0V		0.01	2.0	μA
Reset Voltage	V_{RST}	-	0.4	0.7	1.0	V
Reset Current	I_{RST}	-		0.1	0.4	mA
Low Output Voltage	V_{OL}	V_{CC} = 15V I_{SINK} = 10mA I_{SINK} = 50mA	-	0.06 0.3	0.25 0.75	V V
		V_{CC} = 5V I_{SINK} = 5mA	-	0.05	0.35	V
High Output Voltage	V_{OH}	V_{CC} = 15V I_{SOURCE} = 200mA I_{SOURCE} = 100mA	12.75	12.5 13.3	-	V V
		V_{CC} = 5V I_{SOURCE} = 100mA	2.75	3.3	-	V
Rise Time of Output (Note4)	t_R	-	-	100	-	ns
Fall Time of Output (Note4)	t_F	-	-	100	-	ns
Discharge Leakage Current	I_{LKG}	-	-	20	100	nA

Notes:

1. When the output is high, the supply current is typically 1mA less than at V_{CC} = 5V.
2. Tested at V_{CC} = 5.0V and V_{CC} = 15V.
3. This will determine the maximum value of $R_A + R_B$ for 15V operation, the max. total R = 20MΩ, and for 5V operation, the max. total R = 6.7MΩ.
4. These parameters, although guaranteed, are not 100% tested in production.

Application Information

Table 1 below is the basic operating table of 555 timer:

Table 1. Basic Operating Table

Threshold Voltage (V_{th})(PIN 6)	Trigger Voltage (V_{tr})(PIN 2)	Reset(PIN 4)	Output(PIN 3)	Discharging Tr. (PIN 7)
Don't care	Don't care	Low	Low	ON
V_{th} > 2Vcc / 3	V_{th} > 2Vcc / 3	High	Low	ON
Vcc / 3 < V_{th} < 2 Vcc / 3	Vcc / 3 < V_{th} < 2 Vcc / 3	High	-	-
V_{th} < Vcc / 3	V_{th} < Vcc / 3	High	High	OFF

When the low signal input is applied to the reset terminal, the timer output remains low regardless of the threshold voltage or the trigger voltage. Only when the high signal is applied to the reset terminal, the timer's output changes according to threshold voltage and trigger voltage.

When the threshold voltage exceeds 2/3 of the supply voltage while the timer output is high, the timer's internal discharge Tr. turns on, lowering the threshold voltage to below 1/3 of the supply voltage. During this time, the timer output is maintained low. Later, if a low signal is applied to the trigger voltage so that it becomes 1/3 of the supply voltage, the timer's internal discharge Tr. turns off, increasing the threshold voltage and driving the timer output again at high.

1. Monostable Operation

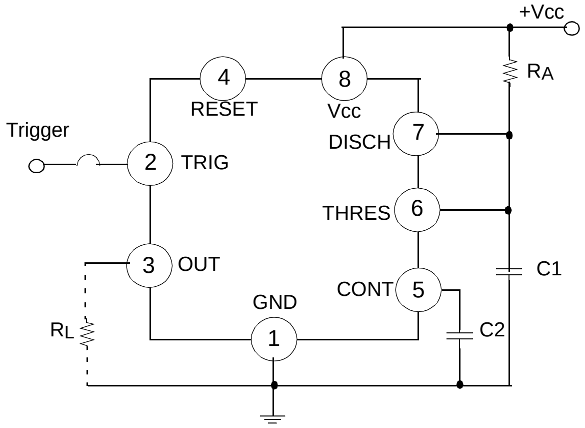


Figure 1. Monoatable Circuit

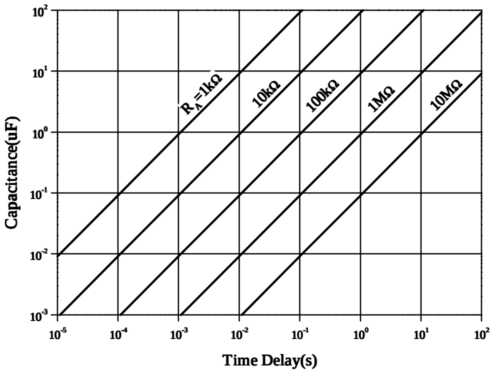


Figure 2. Resistance and Capacitance vs. Time delay(t_d)

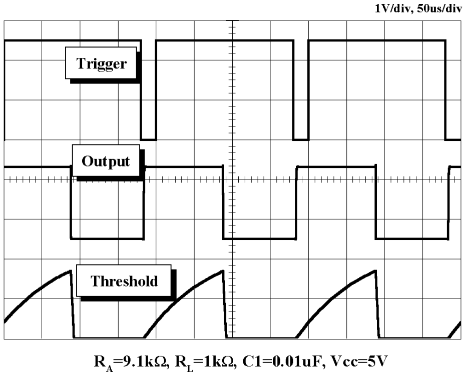
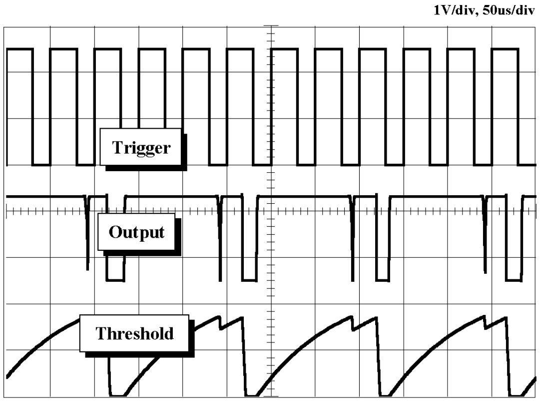


Figure 3. Waveforms of Monostable Operation

Figure 1 illustrates a monostable circuit. In this mode, the timer generates a fixed pulse whenever the trigger voltage falls below Vcc/3. When the trigger pulse voltage applied to the #2 pin falls below Vcc/3 while the timer output is low, the timer's internal flip-flop turns the discharging Tr. off and causes the timer output to become high by charging the external capacitor C1 and setting the flip-flop output at the same time.
The voltage across the external capacitor C1, V_{C1} increases exponentially with the time constant t=R_A*C and reaches 2Vcc/3 at td=1.1R_A*C. Hence, capacitor C1 is charged through resistor R_A. The greater the time constant R_AC, the longer it takes for the V_{C1} to reach 2Vcc/3. In other words, the time constant R_AC controls the output pulse width.
When the applied voltage to the capacitor C1 reaches 2Vcc/3, the comparator on the trigger terminal resets the flip-flop, turning the discharging Tr. on. At this time, C1 begins to discharge and the timer output converts to low.
In this way, the timer operating in the monostable repeats the above process. Figure 2 shows the time constant relationship based on R_A and C. Figure 3 shows the general waveforms during the monostable operation.
It must be noted that, for a normal operation, the trigger pulse voltage needs to maintain a minimum of Vcc/3 before the timer output turns low. That is, although the output remains unaffected even if a different trigger pulse is applied while the output is high, it may be affected and the waveform does not operate properly if the trigger pulse voltage at the end of the output pulse remains at below Vcc/3. Figure 4 shows such a timer output abnormality.



R_A=9.1kΩ, R_L=1kΩ, C1=0.01uF, Vcc=5V

Figure 4. Waveforms of Monostable Operation (abnormal)

2. Astable Operation

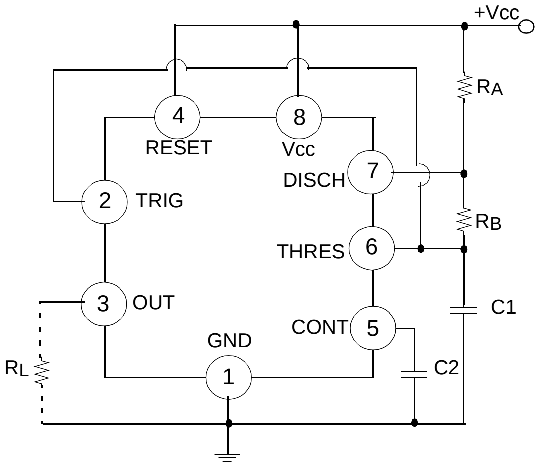


Figure 5. Astable Circuit

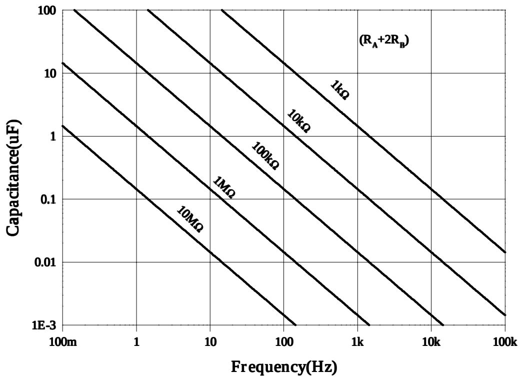
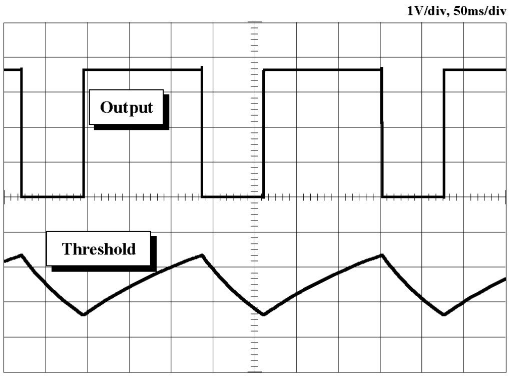


Figure 6. Capacitance and Resistance vs. Frequency



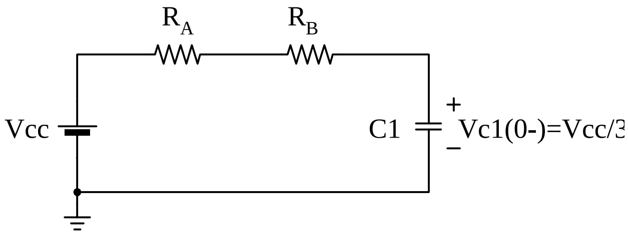
R_A=1kΩ, R_B=1kΩ, R_L=1kW, C1=1uF, Vcc=5V

Figure 7. Waveforms of Astable Operation

An astable timer operation is achieved by adding resistor R_B to Figure 1 and configuring as shown on Figure 5. In the astable operation, the trigger terminal and the threshold terminal are connected so that a self-trigger is formed, operating as a multi vibrator. When the timer output is high, its internal discharging Tr. turns off and the V_{C1} increases by exponential function with the time constant (R_A+R_B)*C.

When the V_{C1}, or the threshold voltage, reaches 2Vcc/3, the comparator output on the trigger terminal becomes high, resetting the F/F and causing the timer output to become low. This in turn turns on the discharging Tr. and the C1 discharges through the discharging channel formed by R_B and the discharging Tr. When the V_{C1} falls below Vcc/3, the comparator output on the trigger terminal becomes high and the timer output becomes high again. The discharging Tr. turns off and the V_{C1} rises again.

In the above process, the section where the timer output is high is the time it takes for the V_{C1} to rise from Vcc/3 to 2Vcc/3, and the section where the timer output is low is the time it takes for the V_{C1} to drop from 2Vcc/3 to Vcc/3. When timer output is high, the equivalent circuit for charging capacitor C1 is as follows:



$$C_1 \frac{dv_{c1}}{dt} = \frac{V_{cc} - V(0-)}{R_A + R_B} \qquad (1)$$

$$V_{C1}(0+) = V_{CC}/3 \qquad (2)$$

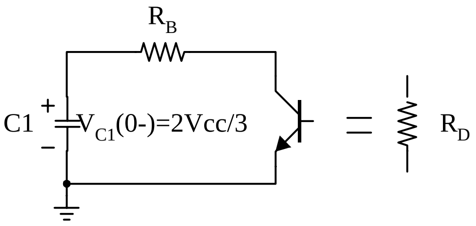
$$V_{C1}(t) = V_{CC}\left(1 - \frac{2}{3} e^{-\left(-\frac{t}{(R_A + R_B)C1}\right)}\right) \qquad (3)$$

Since the duration of the timer output high state(t_H) is the amount of time it takes for the $V_{C1}(t)$ to reach 2Vcc/3,

$$V_{C1}(t) = \frac{2}{3}V_{CC} = V_{CC}\left(1 - \frac{2}{3}e^{-\left(-\frac{t_H}{(R_A + R_B)C1}\right)}\right) \qquad (4)$$

$$t_H = C_1(R_A + R_B)\ln 2 = 0.693(R_A + R_B)C_1 \qquad (5)$$

The equivalent circuit for discharging capacitor C1, when timer output is low is, as follows:



$$C_1\frac{dv_{C1}}{dt} + \frac{1}{R_A + R_B}V_{C1} = 0 \qquad (6)$$

$$V_{C1}(t) = \frac{2}{3}V_{CC}e^{-\frac{t}{(R_A + R_D)C1}} \qquad (7)$$

Since the duration of the timer output low state(t_L) is the amount of time it takes for the V_{C1}(t) to reach Vcc/3,

$$\frac{1}{3}V_{CC} = \frac{2}{3}V_{CC}e^{-\frac{t_L}{(R_A + R_D)C1}} \qquad (8)$$

$$t_L = C_1(R_B + R_D)\ln 2 = 0.693(R_B + R_D)C_1 \qquad (9)$$

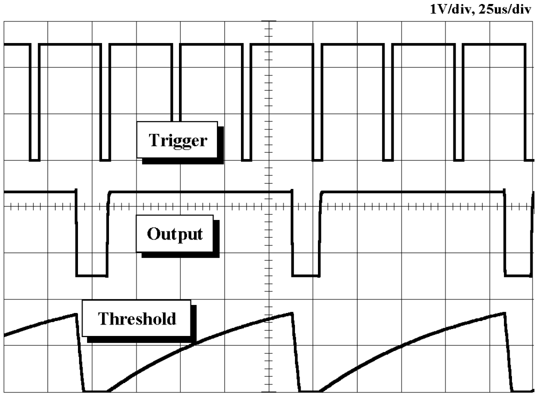
Since R_D is normally $R_B >> R_D$ although related to the size of discharging Tr.,
$t_L = 0.693R_BC_1$ (10)

Consequently, if the timer operates in astable, the period is the same with
'$T = t_H + t_L = 0.693(RA + R_B)C_1 + 0.693R_BC_1 = 0.693(R_A + 2R_B)C_1$' because the period is the sum of the charge time and discharge time. And since frequency is the reciprocal of the period, the following applies.

$$\text{frequency,} \qquad f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C_1} \qquad (11)$$

3. Frequency divider

By adjusting the length of the timing cycle, the basic circuit of Figure 1 can be made to operate as a frequency divider. Figure 8. illustrates a divide-by-three circuit that makes use of the fact that retriggering cannot occur during the timing cycle.

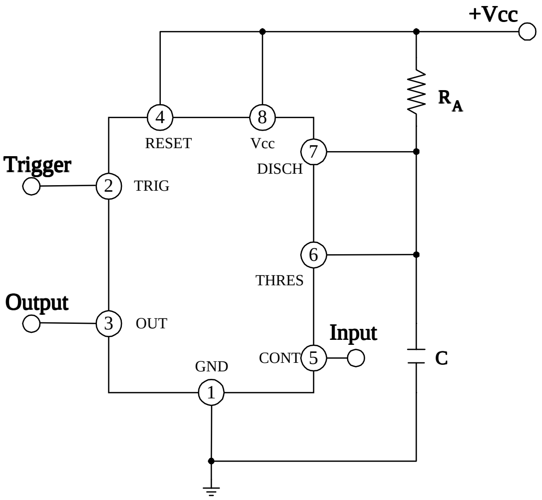


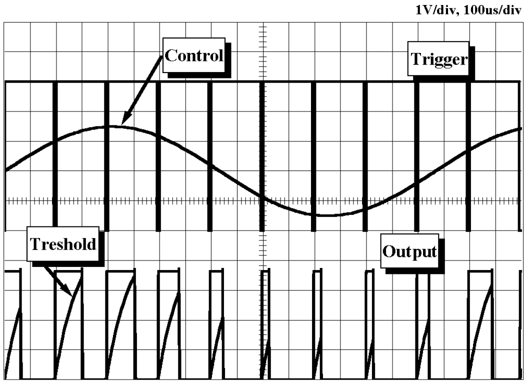
R_A=9.1kΩ, R_L=1kΩ, C1=0.01uF, Vcc=5V

Figure 8. Waveforms of Frequency Divider Operation

4. Pulse Width Modulation

The timer output waveform may be changed by modulating the control voltage applied to the timer's pin 5 and changing the reference of the timer's internal comparators. Figure 9 illustrates the pulse width modulation circuit.
When the continuous trigger pulse train is applied in the monostable mode, the timer output width is modulated according to the signal applied to the control terminal. Sine wave as well as other waveforms may be applied as a signal to the control terminal. Figure 10 shows the example of pulse width modulation waveform.





R_A=9.1kΩ, R_L=1kΩ, C1=0.01uF, Vcc=5V

Figure 9. Circuit for Pulse Width Modulation

Figure 10. Waveforms of Pulse Width Modulation

5. Pulse Position Modulation

If the modulating signal is applied to the control terminal while the timer is connected for the astable operation as in Figure 11, the timer becomes a pulse position modulator.
In the pulse position modulator, the reference of the timer's internal comparators is modulated which in turn modulates the timer output according to the modulation signal applied to the control terminal.
Figure 12 illustrates a sine wave for modulation signal and the resulting output pulse position modulation : however, any wave shape could be used.

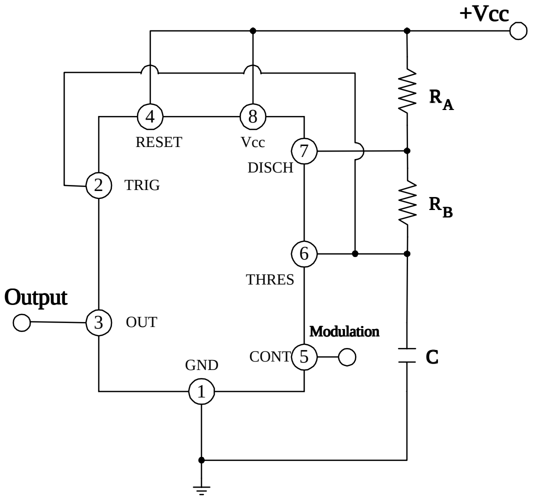
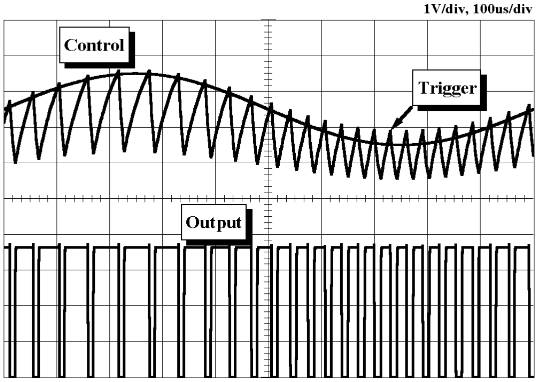


Figure 11. Circuit for Pulse Position Modulation



R_A=3.9kΩ, R_B=1kΩ, R_L=1kΩ, C1=0.01uF, Vcc=5V

Figure 12. Waveforms of pulse position modulation

6. Linear Ramp

When the pull-up resistor RA in the monostable circuit shown in Figure 1 is replaced with constant current source, the V_{C1} increases linearly, generating a linear ramp. Figure 13 shows the linear ramp generating circuit and Figure 14 illustrates the generated linear ramp waveforms.

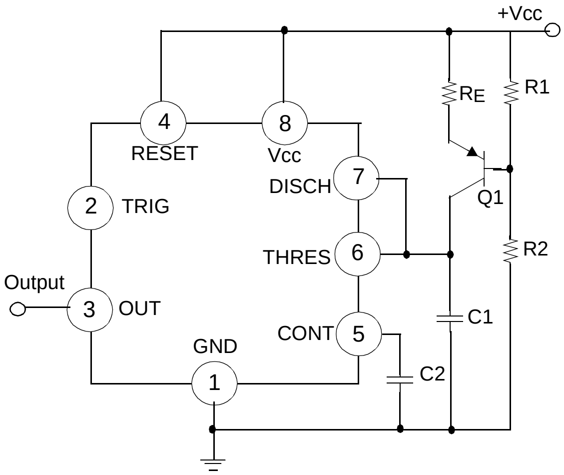
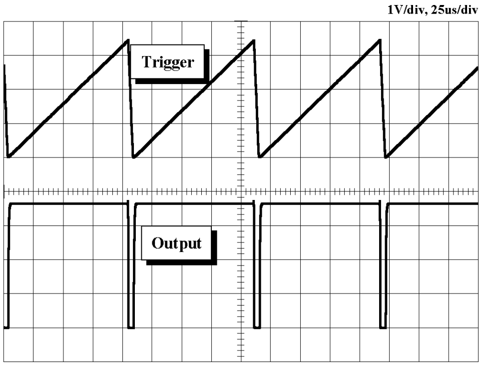


Figure 13. Circuit for Linear Ramp



R1=47kΩ, R2=100kΩ, R_E=2.7kΩ, R_L=1kΩ, C1=0.01uF, Vcc=5V

Figure 14. Waveforms of Linear Ramp

In Figure 13, current source is created by PNP transistor Q1 and resistor R1, R2, and R_E.

$$I_C = \frac{V_{CC} - V_E}{R_E} \qquad (12)$$

Here, V_E is

$$V_E = V_{BE} + \frac{R_2}{R_1 + R_2} V_{CC} \qquad (13)$$

For example, if Vcc=15V, R_E=20kΩ, R1=5kW, R2=10kΩ, and V_{BE}=0.7V,
V_E=0.7V+10V=10.7V
Ic=(15-10.7)/20k=0.215mA

When the trigger starts in a timer configured as shown in Figure 13, the current flowing through capacitor C1 becomes a constant current generated by PNP transistor and resistors.

Hence, the V_C is a linear ramp function as shown in Figure 14. The gradient S of the linear ramp function is defined as follows:

$$S = \frac{V_{p-p}}{T} \qquad (14)$$

Here the Vp-p is the peak-to-peak voltage.

If the electric charge amount accumulated in the capacitor is divided by the capacitance, the V_C comes out as follows:

$$V=Q/C \qquad (15)$$

The above equation divided on both sides by T gives us

$$\frac{V}{T} = \frac{Q/T}{C} \qquad (16)$$

and may be simplified into the following equation.

$$S=I/C \qquad (17)$$

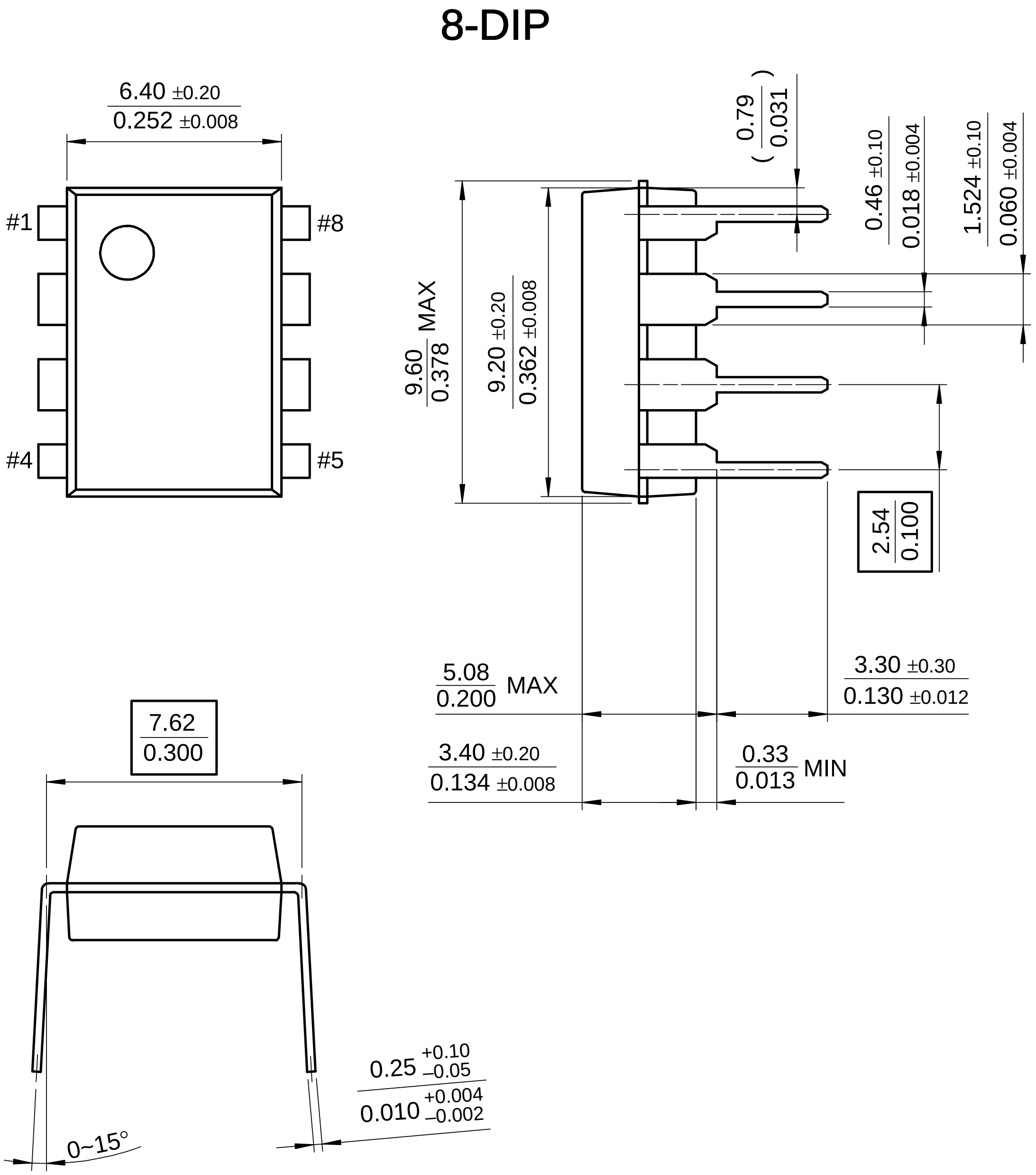
In other words, the gradient of the linear ramp function appearing across the capacitor can be obtained by using the constant current flowing through the capacitor.

If the constant current flow through the capacitor is 0.215mA and the capacitance is 0.02µF, the gradient of the ramp function at both ends of the capacitor is S = 0.215m/0.022µ = 9.77V/ms.

Mechanical Dimensions

Package

Dimensions in millimeters

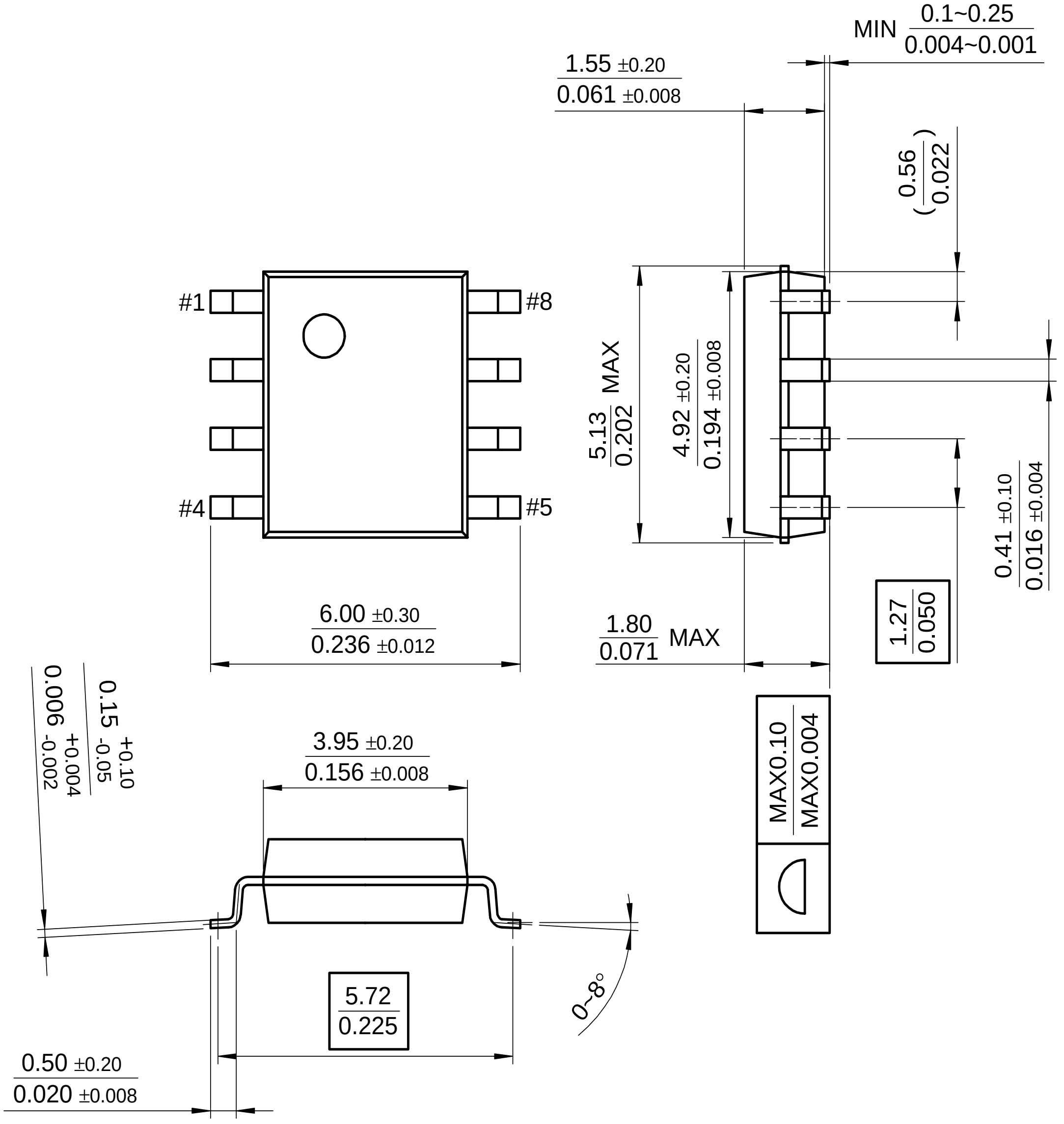


Mechanical Dimensions (Continued)

Package

Dimensions in millimeters

8-SOP



FAIRCHILD
SEMICONDUCTOR®

www.fairchildsemi.com

LM2901,LM339/LM339A,LM3302, LM239/LM239A

Quad Comparator

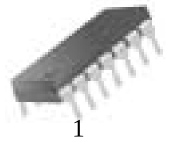
Features

- Single or dual supply operation
- Wide range of supply voltage
  LM2901,LM339/LM339A,LM239/LM239A : 2 ~ 36V (or ±1 ~ ±18V)
  LM3302 : 2 ~ 28V (or ±1 ~ ±14V)
- Low supply current drain 800µA Typ.
- Open collector outputs for wired and connectors
- Low input bias current 25nA Typ.
- Low Input offset current ±2.3nA Typ.
- Low input offset voltage ±1.4mV Typ.
- Common mode input voltage range includes ground.
- Low output saturation voltage
- Output compatible with TTL. DTL and MOS logic system

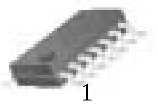
Description

The LM2901, LM339/LM339A ,LM239/LM239A, LM3302 consist of four independent voltage comparators designed to operate from single power supply over a wide voltage range.

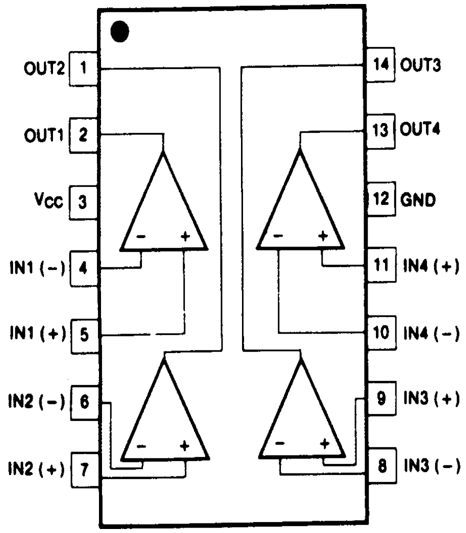
14-DIP



14-SOP

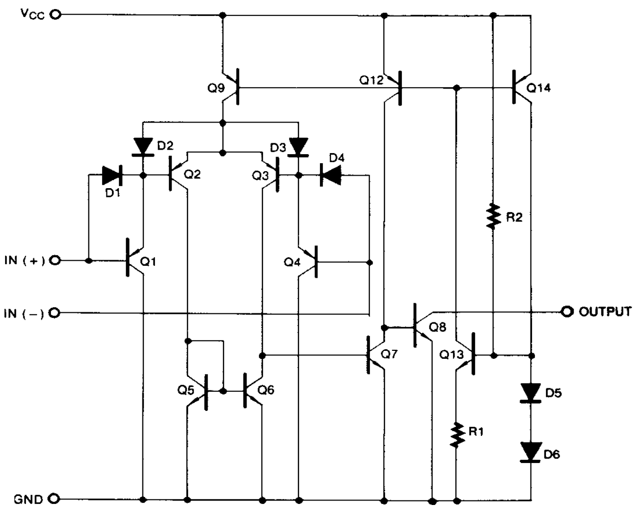


Internal Block Diagram



Rev. 1.0.1

Schematic Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	±18 or 36	V
Supply Voltage only LM3302	V_{CC}	±14 or 28	V
Differential Input Voltage	$V_{I(DIFF)}$	36	V
Differential Input Voltage only LM3302	$V_{I(DIFF)}$	28	V
Input Voltage	V_I	- 0.3 to +36	V
Input Voltage only LM3302	V_I	- 0.3 to +28	V
Output Short Circuit to GND	-	Continuous	-
Power Dissipation	P_D	570	mW
Operating Temperature LM339/LM339A LM2901/LM3302 LM239/LM239A	T_{OPR}	0 ~ + 70 -40 ~ + 85 -25 ~ + 85	°C
Storage Temperature	T_{STG}	- 65 ~ + 150	°C

Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions		LM239A/LM339A			LM239/LM339			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	$V_{O(P)}$ =1.4V, R_S =0Ω		-	±1	±2	-	±1.4	±5	mV
			Note 1	-		±4.0	-	-	±9.0	
Input Offset Current	I_{IO}			-	±2.3	±50	-	±2.3	±50	nA
			Note 1	-		±150	-	-	±150	
Input Bias Current	I_{BIAS}			-	57	250	-	57	250	nA
			Note 1	-	-	400	-	-	400	
Input Common Mode Voltage Range	$V_{I(R)}$			0	-	V_{CC}-1.5	0	-	V_{CC}-1.5	V
			Note 1	0	-	V_{CC}-2	0	-	V_{CC}-2	
Supply Current	I_{CC}	V_{CC} = 5V R_L = ∞		-	1.1	2.0	-	1.1	2.0	mA
Voltage Gain	G_V	V_{CC} =15V, R_L ≥ 15KΩ (for large swing)		50	200	-	50	200	-	V/mV
Large Signal Response Time	T_{LRES}	V_I = TTL Logic Swing V_{REF} = 1.4V, V_{RL} = 5V, R_L = 5.1KΩ		-	350	-	-	350	-	ns
Response Time	T_{RES}	V_{RL} = 5V, R_L = 5.1KΩ		-	1.4	-	-	1.4	-	µs
Output Sink Current	I_{SINK}	$V_{I(-)}$ ≥ 1V, $V_{I(+)}$ = 0V, $V_{O(P)}$ ≤ 1.5V		6	18	-	6	18	-	mA
Output Saturation Voltage	V_{SAT}	$V_{I(-)}$ ≥ 1V, $V_{I(+)}$ = 0V		-	140	400	-	140	400	mV
		I_{SINK} = 4mA	Note 1	-		700	-		700	
Output Leakage Current	$I_{O(LKG)}$	$V_{I(-)}$ = 0V $V_{I(+)}$ = 1V	$V_{O(P)}$ = 5V	-	0.1	-	-	0.1	-	nA
			$V_{O(P)}$ = 30V	-	-	1.0	-	-	1.0	µA
Differential Voltage	$V_{I(DIFF)}$		Note 1	-	-	36	-	-	36	V

Note 1.

LM339/LM339A : 0 ≤ T_A ≤ +70°C

LM2901/LM3302 : -40 ≤ T_A ≤ +85°C

LM239/LM239A : -25 ≤ T_A ≤ +85°C

Electrical Characteristics (Continued)

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions		LM2901			LM3302			Unit
				Min	Typ	Max.	Min	Typ	Max.	
Input Offset Voltage	V_{IO}	$V_{O(P)}$ =1.4V, R_S =0Ω		-	2	7	-	2	20	mV
			Note 1	-	9	15	-	-	40	
Input Offset Current	I_{IO}			-	2.3	50	-	3	100	nA
			Note 1	-	50	200	-	-	300	
Input Bias Current	I_{BIAS}			-	57	250	-	57	250	nA
			Note 1	-	200	500	-	-	1000	
Input Common Mode Voltage Range	$V_{I(R)}$			0	-	V_{CC} -1.5	0	-	V_{CC} -1.5	V
			Note 1	0	-	V_{CC} -2	0	-	V_{CC} -2	
Supply Current	I_{CC}		R_L =∞, V_{CC}=5V	-	1.1	2.0	-	1.1	2.0	mA
			R_L =∞,V_{CC}=30V	-	1.6	2.5	-	-	-	
Voltage Gain	G_V	V_{CC} =15V, R_L ≥ 15KΩ (for large swing)		25	100	-	2	30	-	V/ mV
Large Signal Response Time	T_{LRES}	V_I =TTL Logic Swing V_{REF} =1.4V, V_{RL} =5V, R_L =5.1KΩ		-	350	-	-	350	-	ns
Response Time	T_{RES}	V_{RL} = 5V, R_L = 5.1KΩ		-	1.4	-	-	1.4	-	µs
Output Sink Current	I_{SINK}	$V_{I(-)}$ ≥ 1V, $V_{I(+)}$ =0V, $V_{O(P)}$ ≤ 1.5V		6	18	-	6	18	-	mA
Output Saturation Voltage	V_{SAT}	$V_{I(-)}$ ≥ 1V, $V_{I(+)}$ = 0V		-	140	400	-	140	400	mV
		I_{SINK} =4mA	Note 1	-	-	700	-	-	700	
Output Leakage Current	$I_{O(LKG)}$	$V_{I(-)}$ = 0V $V_{I(+)}$ = 1V	$V_{O(P)}$ = 5V	-	0.1	-	-	0.1	-	nA
			$V_{O(P)}$ = 30V	-	-	1.0	-	-	1.0	µA
Differential Voltage	$V_{I(DIFF)}$		Note 1	-	-	36	-	-	36	V

Note 1.

LM339/LM339A : 0 ≤ T_A ≤ +70°C

LM2901/LM3302 : -40 ≤ T_A ≤ +85°C

LM239/LM239A : -25 ≤ T_A ≤ +85°C

Typical Performance Characteristics

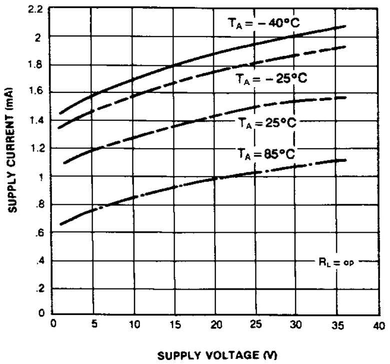


Figure 1. Supply Current vs Supply Voltage

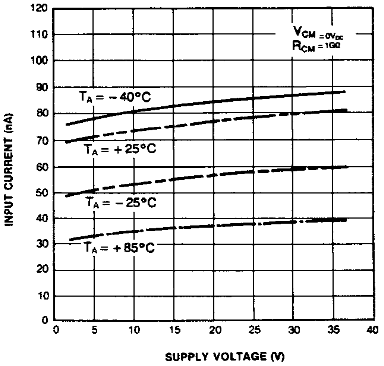


Figure 2. Input Current vs Supply Voltage

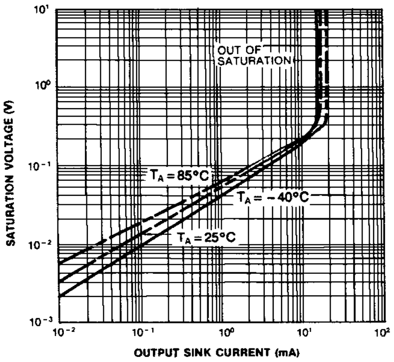


Figure 3. Output Saturation Voltage vs sink Current

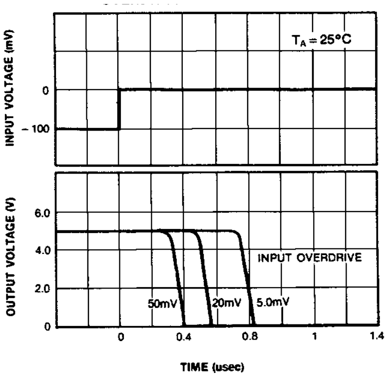


Figure 4. Response Time for Various Input Overdrive-Negative Transition

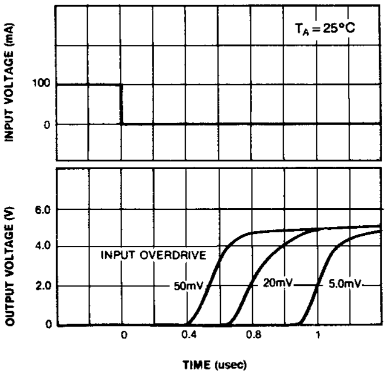
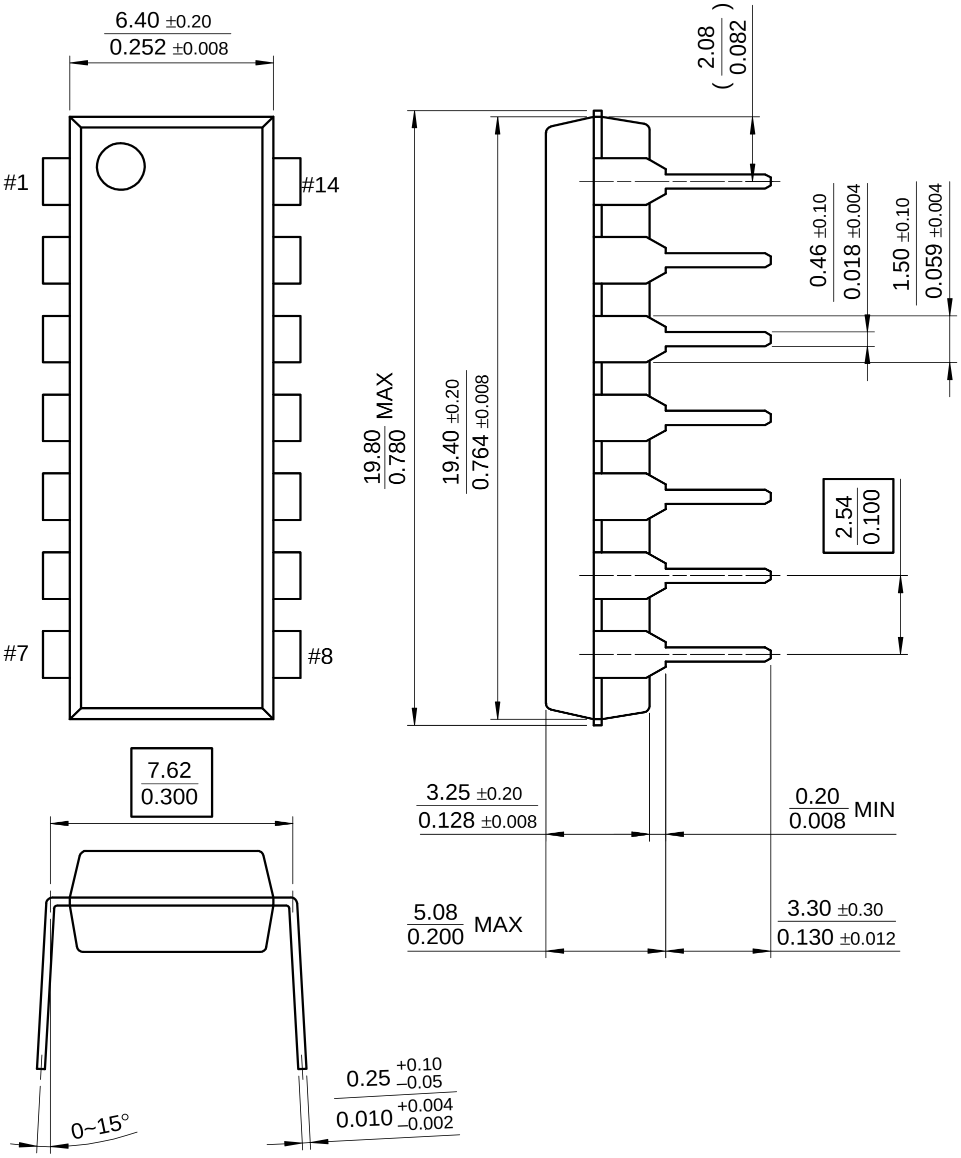


Figure 5. Response Time for Various Input Overdrive-Positive Transition

Mechanical Dimensions

Package

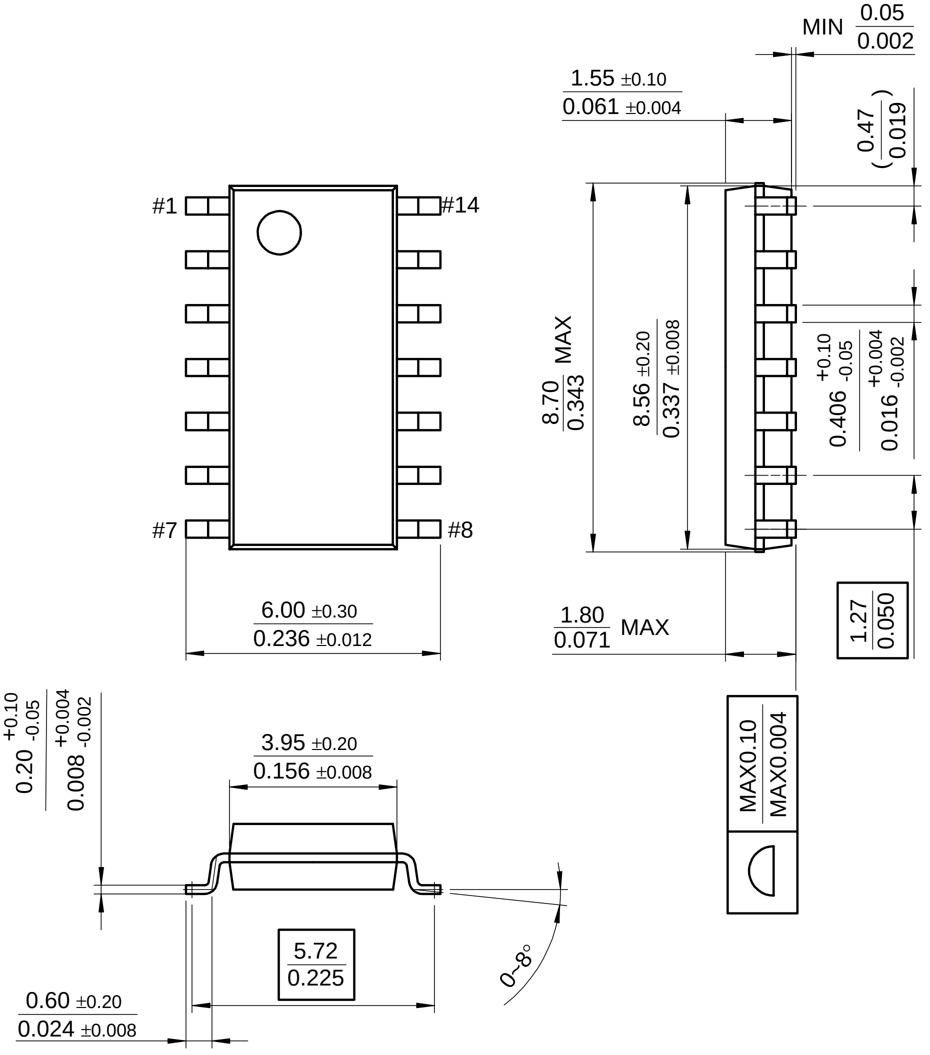
14-DIP



Mechanica Dimensions (Continued)

Package

14-SOP



TIP110/112
TIP115/117

COMPLEMENTARY SILICON POWER DARLINGTON TRANSISTORS

- STMicroelectronics PREFERRED SALESTYPES
- COMPLEMENTARY PNP - NPN DEVICES
- MONOLITHIC DARLINGTON CONFIGURATION
- INTEGRATED ANTIPARALLEL COLLECTOR-EMITTER DIODE

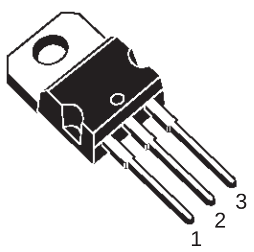
APPLICATIONS

- LINEAR AND SWITCHING INDUSTRIAL EQUIPMENT

DESCRIPTION

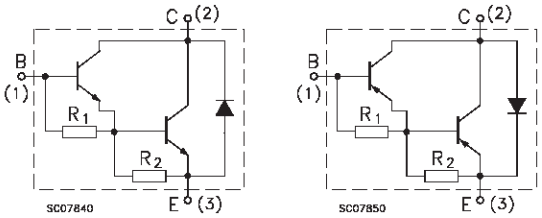
The TIP110 and TIP112 are silicon Epitaxial-Base NPN transistors in monolithic Darlington configuration mounted in Jedec TO-220 plastic package. They are intented for use in medium power linear and switching applications.

The complementary PNP types are TIP115 and TIP117.



TO-220

INTERNAL SCHEMATIC DIAGRAM



R_1 Typ.= 7K Ω R_2 Typ.= 230

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value		Unit
		NPN	TIP110	TIP112	
		PNP	TIP115	TIP117	
V_{CBO}	Collector-Base Voltage ($I_E = 0$)		60	100	V
V_{CEO}	Collector-Emitter Voltage ($I_B = 0$)		60	100	V
V_{EBO}	Emitter-Base Voltage ($I_C = 0$)		5		V
I_C	Collector Current		2		A
I_{CM}	Collector Peak Current		4		A
I_B	Base Current		50		mA
P_{tot}	Total Dissipation at $T_{case} \le 25$ °C		50		W
	$T_{amb} \le 25$ °C		2		W
T_{stg}	Storage Temperature		-65 to 150		°C
T_j	Max. Operating Junction Temperature		150		°C

* For PNP types voltage and current values are negative

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	2.5	$^oC/W$
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	62.5	$^oC/W$

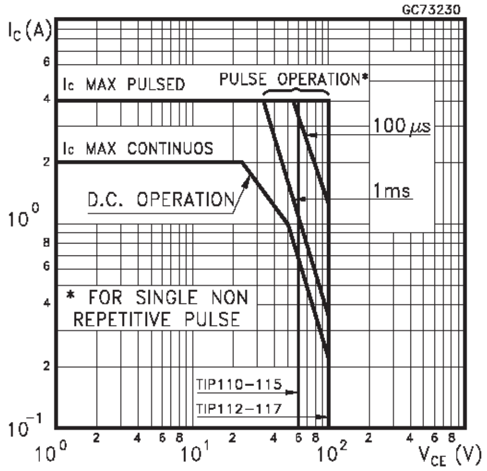
ELECTRICAL CHARACTERISTICS (T_{case} = 25 ^oC unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CEO}	Collector Cut-off Current (I_B = 0)	V_{CE} = Half Rated V_{CEO}			2	mA
I_{CBO}	Collector Cut-off Current (I_E = 0)	V_{CB} = Rated V_{CBO}			1	mA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 5 V			2	mA
$V_{CEO(sus)}$*	Collector-Emitter Sustaining Voltage (I_B = 0)	I_C = 30 mA for **TIP110/115** for **TIP112/117**	 60 100			 V V
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 2 A I_B = 8 mA			2.5	V
V_{BE}*	Base-Emitter Voltage	I_C = 2 A V_{CE} = 4 V			2.8	V
h_{FE}*	DC Current Gain	I_C = 1 A V_{CE} = 4 V I_C = 2 A V_{CE} = 4 V	1000 500			

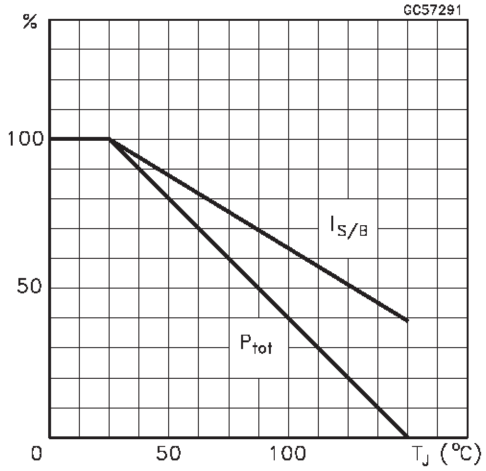
∗ Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

For PNP types voltage and current values are negative.

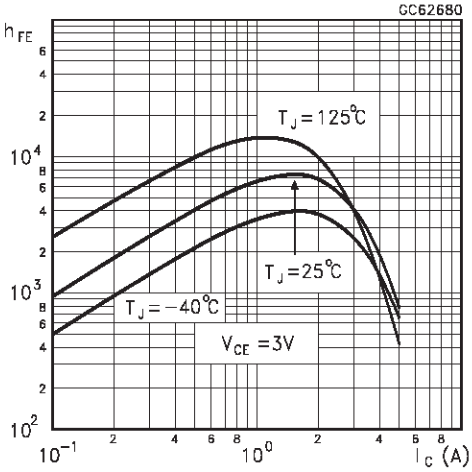
Safe Operating Areas



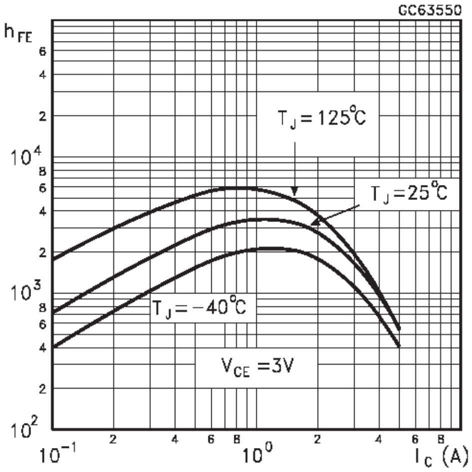
Derating Curve



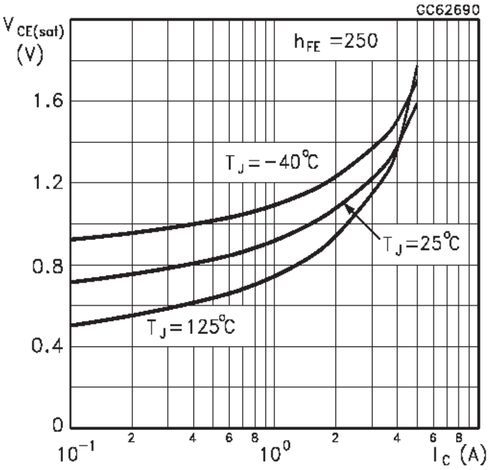
DC Current Gain (NPN type)



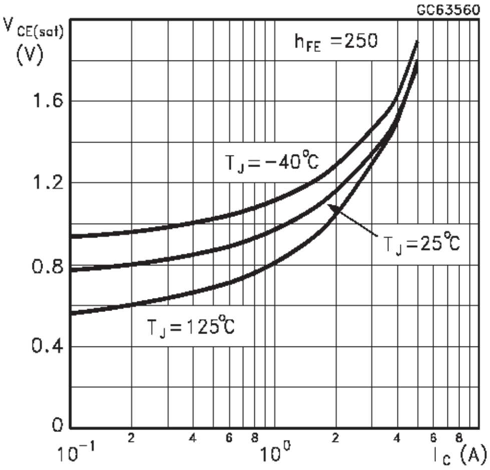
DC Current Gain (PNP type)



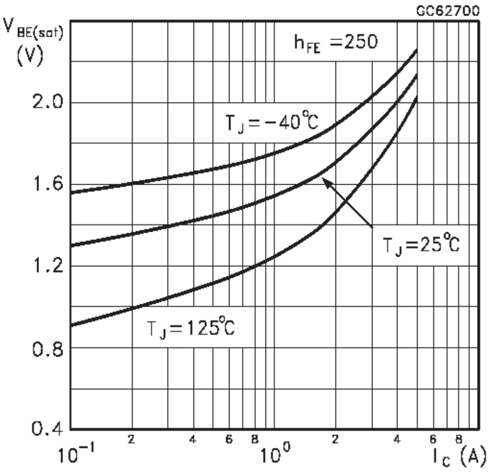
Collector-Emitter Saturation Voltage (NPN type)



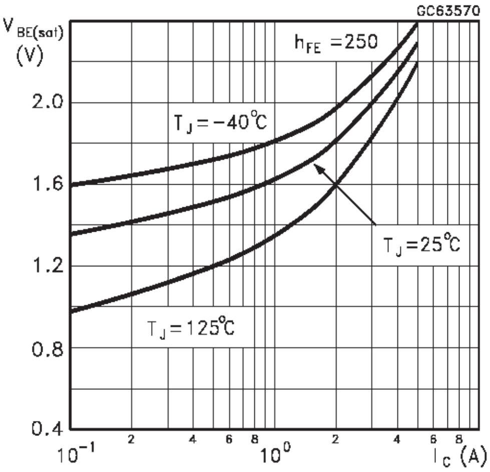
Collector-Emitter Saturation Voltage (PNP type)



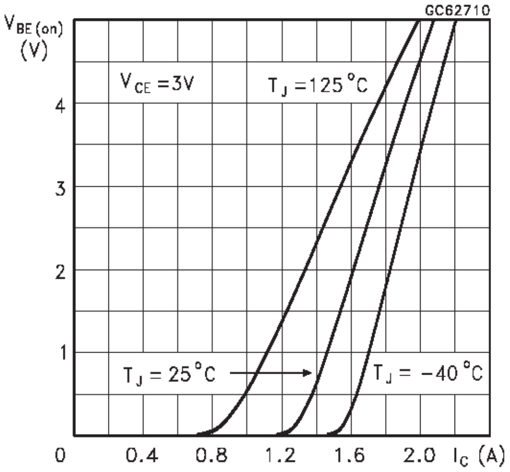
Base-Emitter Saturation Voltage (NPN type)



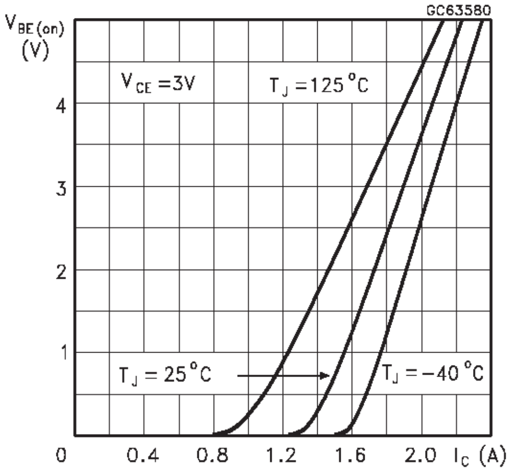
Base-Emitter Saturation Voltage (PNP type)



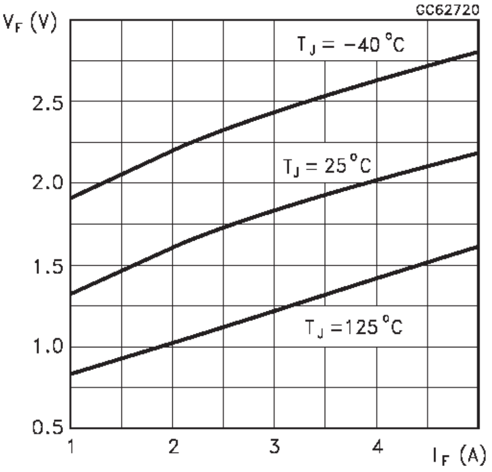
Base-Emitter On Voltage (NPN type)



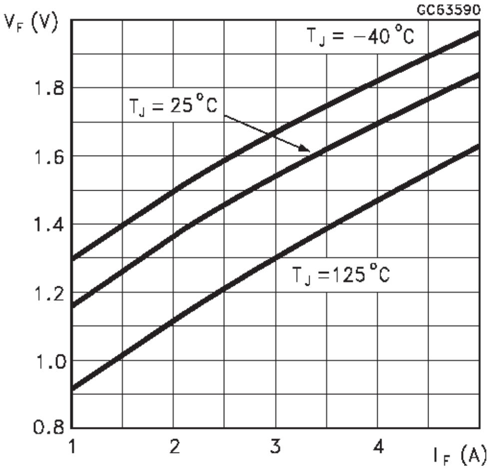
Base-Emitter On Voltage (PNP type)



Freewheel Diode Forward Voltage (NPN types)



Freewheel Diode Forward Voltage (PNP types)



TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151